Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of facilitating testing of a first module and a second module together in an integrated circuit, said method comprising:
providing said second module with a capability of being tested in each of a plurality of characteristics of a first control signal;
providing a programmable field, which can be programmed to generate a derived control signal having a desired characteristic, wherein said derived control signal is generated from said first control signal by programming said programmable field,
wherein said derived control signal of said desired characteristic is provided as a control signal to said second module and said second module is tested with said desired characteristic of said first control signal by programming said programmable field.

[c2] 2. The method of claimwherein said desired characteristic is determined to test a path connecting said first module and said second module at a same speed as in a functional mode of operation of said integrated circuit.

[c3] 3. The method of claim 2, wherein said first control sig-

nal comprises a clock signal, and wherein said programmable field can be set to generate said derived control signal as an inverted signal of said clock signal.

[c4] 4. The method of claim 2, wherein said first control signal comprises a scan enable signal and wherein said programmable field can be set to generate said derived control signal as rising edge triggered or falling edge triggered scan enable signal.

[c5] 5. The method of claim 2, wherein said programmable field comprises a register.

[c6] 6. The method of claim 2, wherein said first module comprises a core module provided by a third party not designing said integrated circuit, and said second module is designed by a designer designing said integrated circuit.

[c7] 7. An integrated circuit designed for testing of a first module, wherein said first module is to be integrated into said integrated circuit, said integrated circuit comprising:

a second module provided with a capability of being tested in each of a plurality of characteristics of a first control signal, said second module being coupled to said first module by at least one path;

a test logic being programmable to generate a derived control signal having a desired characteristic, wherein said derived control signal is generated from said first control signal, and

wherein said derived control signal of said desired characteristic is provided as a control signal to said second module and said second module is tested with said desired characteristic of said first control signal by programming said test logic.

[c8] 8. The integrated circuit of claimwherein said desired characteristic is determined to test said path at a same speed as in a functional mode.

[c9] 9. The integrated circuit of claim 8, wherein said first control signal comprises a clock signal, and wherein said test logic can be programmed to generate said derived control signal as an inverted signal of said clock signal.

[c10] 10. The integrated circuit of claim 9, wherein said test logic comprises:

a bit indicating whether said derived control signal is to be generated as a positive clock signal or a negative clock signal; and

an XOR logic gate receiving said bit and said clock signal and generating said derived control signal.

[c11] 11. The integrated circuits of claim 8, wherein said first control signal comprises a scan enable signal and wherein said programmable field can be set to generate said derived control signal as rising edge triggered or falling edge triggered scan enable signal.

[c12] 12. The integrated circuit of claim 11, wherein said test logic comprises:
a bit indicating whether said derived clock signal is to be generated as said rising edge triggered or said falling edge triggered scan enable signal;
a flip-flop coupled to receive said original control signal and being clocked on an inverted clock signal; and
a multiplexor selecting either the output of said flip-flop or said original control signal under the control of said bit.

[c13] 13. The integrated circuit of claim 8, wherein said test logic comprises a register which can be programmed.

[c14] 14. The integrated circuit of claim 8, wherein said first module comprises a core module provided by a third party not designing said integrated circuit, and said second module is designed by a designer designing said integrated circuit.